

WHAT IS CLAIMED IS:

- 1 1. A capacitor comprising:
2 a strained semiconductor layer;
3 a bottom electrode formed in a portion of the strained semiconductor layer;
4 a capacitor dielectric overlying the bottom electrode;
5 a top electrode overlying the capacitor dielectric; and
6 at least one bottom electrode contact region formed in the strained semiconductor layer
7 adjacent the bottom electrode, the at least one bottom electrode contact region being doped to a
8 first conductivity type wherein the bottom electrode is operationally the first conductivity type.
- 1 2. The capacitor of claim 1 wherein the capacitor is a decoupling capacitor.
- 1 3. The capacitor of claim 2 wherein the top electrode is connected to a power supply line
2 and the bottom electrode is connected to a ground line.
- 1 4. The capacitor of claim 2 wherein the top electrode is connected to a first power supply
2 line and the bottom electrode is connected to a second power supply line.
- 1 5. The capacitor of claim 1 wherein the bottom electrode is substantially flat.
- 1 6. The capacitor of claim 1 further comprising an isolation region adjacent to bottom
2 electrode.
- 1 7. The capacitor of claim 6 wherein the isolation region is shallow trench isolation.

- 1 8. The capacitor of claim 1 wherein the top electrode is substantially flat.
- 1 9. The capacitor of claim 1 wherein the strained semiconductor layer comprises a strained
2 silicon layer.
- 1 10. The capacitor of claim 9 and further comprising a silicon germanium layer underlying the
2 strained silicon layer.
- 1 11. The capacitor of claim 10 wherein the silicon germanium layer has a germanium
2 concentration in the range of about 10 to about 90%.
- 1 12. The capacitor of claim 11 wherein the silicon germanium layer has a germanium
2 concentration in the range of about 20 to about 40%.
- 1 13. The capacitor of claim 1 wherein the semiconductor layer comprises of silicon and
2 germanium.
- 1 14. The capacitor of claim 1 and further comprising an insulator layer underlying the strained
2 semiconductor layer.
- 1 15. The capacitor of claim 14 wherein the insulator layer comprises silicon oxide.
- 1 16. The capacitor of claim 14 wherein the insulator layer has a thickness of less than about
2 1200 angstroms.
- 1 17. The capacitor of claim 14 wherein the bottom electrode is isolated from adjacent
2 elements by mesa isolation.

1 18. The capacitor of claim 14 wherein the semiconductor layer has a thickness in the range of
2 about 20 angstroms to about 500 angstroms.

1 19. The capacitor of claim 1 wherein the top electrode comprises a material selected from the
2 group consisting of poly-crystalline silicon and poly-crystalline silicon-germanium.

1 20. The capacitor of claim 1 wherein the top electrode comprises a material selected from the
2 group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 21. The capacitor of claim 1 wherein the top electrode comprises a material selected from the
2 group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and
3 combinations thereof.

1 22. The capacitor of claim 1 wherein the top electrode comprises a material selected from the
2 group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum
3 silicide, platinum silicide, erbium silicide, and combinations thereof.

1 23. The capacitor of claim 1 wherein the top electrode comprises a material selected from the
2 group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

1 24. The capacitor of claim 1 wherein the capacitor dielectric comprises a high permittivity
2 dielectric.

1 25. The capacitor of claim 24 wherein the high permittivity dielectric is selected from the
2 group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
3 zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

- 1 26. The capacitor of claim 24 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 10.
- 1 27. The capacitor of claim 24 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 20.
- 1 28. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 10 angstroms.
- 1 29. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 50 angstroms.
- 1 30. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 100 angstroms.
- 1 31. The capacitor of claim 1 wherein the capacitor has a width of larger than about 5
2 microns.
- 1 32. The capacitor of claim 1 wherein the capacitor has a width of larger than about 10
2 microns.
- 1 33. The capacitor of claim 1 wherein the capacitor has a length of larger than about 1 micron.
- 1 34. The capacitor of claim 1 wherein the capacitor has a length of larger than about 5
2 microns.

- 1 35. The capacitor of claim 1 wherein the bottom electrode is physically doped to a first
2 conductivity type and the bottom electrode contact region is physically doped to a second
3 conductivity type.
- 1 36. The capacitor of claim 35 wherein the first conductivity type is n-type and the second
2 conductivity type is p-type.
- 1 37. The capacitor of claim 35 wherein the first conductivity type is p-type and the second
2 conductivity type is n-type.
- 1 38. The capacitor of claim 1 wherein the bottom electrode is physically doped to a first
2 conductivity type and the bottom electrode contact region is physically doped to the first
3 conductivity type.
- 1 39. The capacitor of claim 1 and further comprising spacers formed on the sides of the top
2 electrode.
- 1 40. The capacitor of claim 39 wherein the spacers comprise silicon nitride.
- 1 41. The capacitor of claim 39 and further comprising an etch-stop layer overlying the top
2 electrode and the spacers.
- 1 42. The capacitor of claim 41 wherein the etch-stop layer comprises silicon nitride.
- 1 43. The capacitor of claim 41 and further comprising an inter-layer dielectric overlying the
2 etch-stop layer.

- 1 44. The capacitor of claim 43 wherein the inter-layer dielectric comprises silicon oxide.
- 1 45. The capacitor of claim 43 wherein the inter-layer dielectric comprises a dielectric with a
2 relative permittivity smaller than about 3.5.
- 1 46. The capacitor of claim 43 wherein the inter-layer dielectric comprises a dielectric with a
2 relative permittivity smaller than about 3.0.
- 1 47. The capacitor of claim 43 wherein the inter-layer dielectric is selected from the group
2 consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen
3 silsesquioxane (HSQ), and SiOF.
- 1 48. The capacitor of claim 43 further comprising a first contact plug in electrical contact with
2 the bottom electrode and a second contact plug in electrical contact with the top electrode.

1 49. A decoupling capacitor comprising:
2 a semiconductor substrate including a strained silicon layer,
3 a substantially flat bottom electrode formed in a portion of the strained silicon layer;
4 a capacitor dielectric overlying the bottom electrode;
5 a substantially flat top electrode overlying said capacitor dielectric;
6 wherein the top electrode is connected to a first reference voltage line and the bottom
7 electrode is connected to a second reference voltage line.

1 50. The capacitor of claim 49 wherein the top electrode is connected to a power supply line
2 and the bottom electrode is connected to a ground line.

1 51. The capacitor of claim 49 wherein the top electrode is connected to a first power supply
2 line and the bottom electrode is connected to a second power supply line.

1 52. The capacitor of claim 49 wherein the semiconductor substrate further comprises a
2 silicon germanium layer underlying the strained silicon layer.

1 53. The capacitor of claim 49 wherein the semiconductor substrate further comprises an
2 insulator layer underlying the strained silicon layer.

1 54. The capacitor of claim 49 wherein the top electrode comprises a material selected from
2 the group consisting of poly-crystalline silicon and poly-crystalline silicon-germanium.

1 55. The capacitor of claim 49 wherein the top electrode comprises a material selected from
2 the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 56. The capacitor of claim 49 wherein the top electrode comprises a material selected from
2 the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride,
3 and combinations thereof.

1 57. The capacitor of claim 49 wherein the top electrode comprises a material selected from
2 the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,
3 tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

1 58. The capacitor of claim 49 wherein the top electrode comprises a material selected from
2 the group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

1 59. The capacitor of claim 49 wherein the capacitor dielectric comprises a high permittivity
2 dielectric.

1 60. The capacitor of claim 59 wherein the high permittivity dielectric is selected from the
2 group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
3 zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

1 61. The capacitor of claim 59 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 10.

1 62. The capacitor of claim 59 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 20.

1 63. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 10 angstroms.

1 64. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 50 angstroms.

1 65. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 100 angstroms.

1 66. The capacitor of claim 49 wherein the capacitor has a width of larger than about 5
2 microns.

1 67. The capacitor of claim 49 wherein the capacitor has a width of larger than about 10
2 microns.

1 68. The capacitor of claim 49 wherein the capacitor has a length of larger than about 1
2 micron.

1 69. The capacitor of claim 49 wherein the capacitor has a length of larger than about 5
2 microns.

1 70. The capacitor of claim 49 wherein the bottom electrode has a first conductivity type and
2 wherein the capacitor further comprises at least one doped region of a second conductivity type
3 located within the strained silicon layer adjacent the bottom electrode.

1 71. The capacitor of claim 70 wherein the first conductivity type is n-type and the second
2 conductivity type is p-type.

1 72. The capacitor of claim 70 wherein the first conductivity type is p-type and the second
2 conductivity type is n-type.

1 73. The capacitor of claim 49 wherein the bottom electrode has a first conductivity type and
2 wherein the capacitor further comprises at least one doped region of the first conductivity type
3 located with the strained silicon layer adjacent the bottom electrode.

1 74. The capacitor of claim 49 and further comprising an etch-stop layer overlying the top
2 electrode.

1 75. The capacitor of claim 74 wherein the etch-stop layer comprises silicon nitride.

1 76. The capacitor of claim 74 and further comprising an inter-layer dielectric overlying the
2 etch-stop layer, wherein the inter-layer dielectric comprises a dielectric with a relative
3 permittivity smaller than about 3.5.

1 77. The capacitor of claim 76 wherein the inter-layer dielectric comprises a dielectric with a
2 relative permittivity smaller than about 3.0.

1 78. The capacitor of claim 76 wherein the inter-layer dielectric is selected from the group
2 consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen
3 silsesquioxane (HSQ), and SiOF.

1 79. The capacitor of claim 76 further comprising a first contact plug in electrical contact with
2 the bottom electrode and a second contact plug in electrical contact with the top electrode.

1 80. The capacitor of claim 49 further comprising a shallow trench isolation region adjacent to
2 bottom electrode.

1 81. The capacitor of claim 49 wherein the bottom electrode is isolated by mesa isolation.

1 82. A method of forming a capacitor, the method comprising:
2 providing a semiconductor substrate including a strained silicon layer;
3 forming a bottom electrode in the strained silicon layer;
4 forming a capacitor dielectric on bottom electrode;
5 forming a top electrode on capacitor dielectric;
6 forming a bottom electrode contact region within the strained silicon layer adjacent the
7 bottom electrode; and
8 electrically connecting the bottom electrode and the bottom electrode contact region.

1 83. The method of claim 82 wherein the capacitor is a decoupling capacitor, the method
2 further comprising connecting the bottom electrode to a first reference node and connecting the
3 top electrode to a second reference node.

1 84. The method of claim 82 wherein forming the bottom electrode comprises:
2 forming an active region;
3 forming isolation regions surrounding the active region; and
4 doping the active region to form a bottom electrode.

1 85. The method of claim 84 wherein the active region has a doping concentration of larger
2 than about 10^{19} cm^{-3} .

1 86. The method of claim 82 wherein forming the capacitor dielectric comprises a chemical
2 vapor deposition step or sputter deposition step.

- 1 87. The method of claim 82 wherein the step of forming the capacitor dielectric comprises:
2 forming an interfacial oxide layer; and
3 forming a high permittivity dielectric layer.
- 1 88. The method of claim 82 wherein forming bottom electrode contact region comprises:
2 doping a portion of the strained silicon layer not covered by top electrode;
3 forming spacers on sides of the top electrode; and
4 doping a portion of the silicon layer not covered by the top electrode and spacers.
- 1 89. The method of claim 88 wherein the spacers comprise silicon nitride.
- 1 90. The method of claim 88 further comprising:
2 depositing an etch-stop layer over top electrode and spacers;
3 forming an inter-layer dielectric over etch-stop layer;
4 forming contact holes in inter-layer dielectric; and
5 filling the contact holes with a conductive material to form contact plugs.
- 1 91. The method of claim 90 wherein the etch-stop layer comprises silicon nitride.
- 1 92. The method of claim 90 wherein the inter-layer dielectric comprises silicon oxide.
- 1 93. The method of claim 90 wherein the inter-layer dielectric comprises a dielectric with a
2 relative permittivity smaller than about 3.5.
- 1 94. The method of claim 90 wherein the inter-layer dielectric comprises a dielectric with a
2 relative permittivity smaller than about 3.0.

1 95. The method of claim 90 wherein the inter-layer dielectric is selected from the group
2 consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen
3 silsesquioxane (HSQ), and SiOF.

1 96. The method of claim 90 wherein filling the contact holes comprises forming a first
2 contact plug that electrically contacts the bottom electrode and forming a second contact plug
3 that electrically contacts the top electrode.

1 97. The method of claim 96 wherein the top electrode is connected to a power supply line
2 and the bottom electrode is connected to a ground line.

1 98. The method of claim 96 wherein the top electrode is connected to a first power supply
2 line and the bottom electrode is connected to a second power supply line.

1 99. The method of claim 82 wherein the semiconductor substrate further comprises a silicon
2 germanium layer underlying the strained silicon layer.

1 100. The method of claim 99 wherein the silicon germanium layer has a germanium
2 concentration in the range of about 10 to about 90%.

1 101. The method of claim 99 wherein the silicon germanium layer has a germanium
2 concentration in the range of about 20 to about 40%.

1 102. The method of claim 82 wherein the semiconductor substrate further comprises an
2 insulator layer underlying the strained silicon layer.

- 1 103. The method of claim 102 wherein the insulator layer comprises silicon oxide.
- 1 104. The method of claim 102 wherein the insulator layer has a thickness of less than about
2 1200 angstroms.
- 1 105. The method of claim 82 wherein the strained silicon layer has a thickness in the range of
2 about 20 angstroms to about 500 angstroms.
- 1 106. The method of claim 82 wherein the top electrode comprises poly-crystalline silicon or
2 poly-crystalline silicon-germanium.
- 1 107. The method of claim 82 wherein the top electrode is selected from the group consisting
2 of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.
- 1 108. The method of claim 82 wherein the top electrode is selected from the group consisting
2 of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations
3 thereof.
- 1 109. The method of claim 82 wherein the top electrode is selected from the group consisting
2 of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum
3 silicide, erbium silicide, and combinations thereof.
- 1 110. The method of claim 82 wherein the top electrode is selected from the group consisting
2 of ruthenium oxide, indium tin oxide, and combinations thereof.

1 111. The method of claim 82 wherein the capacitor dielectric comprises a high permittivity
2 dielectric.

1 112. The method of claim 111 wherein the high permittivity dielectric is selected from the
2 group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
3 zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

1 113. The method of claim 111 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 10.

1 114. The method of claim 111 wherein the high permittivity dielectric has a relative
2 permittivity of larger than about 20.

1 115. The method of claim 82 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 10 angstroms.

1 116. The method of claim 82 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 50 angstroms.

1 117. The method of claim 82 wherein the capacitor dielectric has a physical thickness of
2 smaller than about 100 angstroms.

1 118. The method of claim 82 wherein the capacitor has a width of larger than about 5 microns.

1 119. The method of claim 82 wherein the capacitor has a width of larger than about 10
2 microns.

1 120. The method of claim 82 wherein the capacitor has a length of larger than about 1 micron.

1 121. The method of claim 82 wherein the capacitor has a length of larger than about 5 microns